



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/788,582	02/16/2001	John Susantha Fernando	9-11-4	8752

7590 11/28/2005

Ryan, Mason & Lewis, LLP
Suite 205
1300 Post Road
Fairfield, CT 06430

EXAMINER

CAO, CHUN

ART UNIT PAPER NUMBER

2115

DATE MAILED: 11/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.



UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Application Number: 09/788,582
Filing Date: February 16, 2001
Appellant(s): FERNANDO ET AL.

MAILED
NOV 28 2005
Technology Center 2100

Kevin M. Mason
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 9/12/05 appealing from the Office action mailed 5/12/05.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

No evidence is relied upon by the examiner in the rejection of the claims under appeal.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-23 and are rejected under 35 U.S.C. 102(b) as being anticipated by Tateishi (Tateishi), U.S. patent no. 5,539,590. This rejection is set forth in prior Office Action, Paper No. 20050509, and is reproduced below:

Appellant did not separately argue the dependent claims. There are three independent claims, namely claims 1, 8 and 16. Independent claims 1 and 8 are method claim. Claim 8 is written in means plus function and contained the same limitations as claim 1. Independent claim 16 is an apparatus claim corresponding the method claim 1. Claim 1 therefore is selected as an exemplary in the rejection below.

Attention of the Board is respectfully directed to Figure 3 and the corresponding description in Tateishi. With respect to claim 1, Tateishi teaches:

The method of the invention comprising:

adjusting a voltage level of the control signal [STS, fig. 4] from a previous time interval to indicate a first signal state [change of floppy status – from loaded to unloaded or unloaded to loaded; see col. 7, lines 30 – 43, col. 8, lines 49 – 50]; and

maintaining said voltage level of said control signal from the previous time interval to indicate a second signal state [no change of the floppy status].

Specifically, the control signal STS is inputted to the delay FF [DFF] and the EXCLUSIVE-OR gate EX1 [fig. 3]. The output of DFF is connected to the other input of EX1. When there is no change of the floppy status [When the floppy is in the floppy drive, the STS signal is high. The signal STS is maintained at the high level as long as the floppy is in the floppy drive. When the floppy is not in the floppy drive, the STS

Art Unit: 2115

signal is low. The signal STS is maintained at the low level as long as the floppy is not in the floppy drive. [see fig. 4], the two inputs of the EX1 are either both 1 or 0 and the output of EX1 is 0 indicating a second signal state- no change of the floppy status [The floppy is either continuously inside or outside the floppy drive]. Where there is a change of floppy status [The STS signal changes from either high to low or low to high depending upon whether the floppy is unloaded or loaded into the floppy drive], the two inputs of the EX1 are 1 or 0 respectively and the output of EX1 is 1 indicating a first signal state – change of floppy status [col. 7, lines 16 – col. 8 line 51, col. 12, lines 31-38].

(10) Response to Argument

In the Appeal Brief, Appellant argued in substance that Tateishi teaches: (1) STS has two states – load state (STS is high, floppy disk is inside the drive) and unload state (STS is low, no floppy disk is inside the drive); (2) the output of EX1 does not maintain the voltage of a control signal to indicate no change of the floppy status.

Examiner agrees with Appellant's positions. However, the examiner submits that Appellant argument is misplaced. The examiner defined the two signal states as (1) there is a change of floppy status (floppy disk is inserted into the drive or floppy disk is removed from the drive), (2) there is no change in floppy drive status (floppy is either inside or outside the floppy drive). STS, not the output of EX1, is used to indicate the two signal states.

Art Unit: 2115

STS represents the two signal states:

1. There is a change of floppy drive status – the STS is changing from high to low or low to high – adjusting the voltage level from a previous time interval
2. There is no change in floppy drive status - the STS is either stays high or low - maintaining the voltage level from the previous time interval

When the floppy disk is being removed from the drive, the STS changes the voltage from high to low indicating there is a change of state (the claimed state 1). So long as the floppy disk remains outside the drive, the STS maintains the current low voltage level indicating there is no change of state (the claimed state 2). When the floppy disk is being inserted into the drive, the STS changes the voltage from low to high indicating there is a change of state (the claimed state 1). So long as the floppy disk remains inside the drive, the STS maintains the current high voltage level indicating there is no change of state (the claimed state 2).

Appellant position	Examiner position
disk drive has two signal states	disk drive has two signal states
state 1 – floppy disk is inside the drive and the STS is high	state 1 – there is a change in the drive state, the STS adjusts the voltage from high to low or low to high
state 2 – floppy disk is outside the drive and the STS is low	state 2 – there is no change in the drive state, the floppy disk is either inside or outside the drive, STS maintains the voltage in either high or low

Claimed invention	Examiner position
control signal has two signal states	STS has two signal states
state 1 – adjusting the voltage level from a previous signal state	state 1 –STS adjusts the voltage from high to low or low to high
state 2 – maintaining the voltage level from a previous signal state	state 2 –STS maintains the voltage in either high or low

Art Unit: 2115

In summary, Tateishi meets all the claim limitations as shown in the rejection above; furthermore, Tateishi discloses that a memory element [DFF, fig. 3] for maintained a voltage level from a previous time interval [col. 6, lines 11-18] as cited in claim 16.

(11) Related Proceeding(s) Appendix

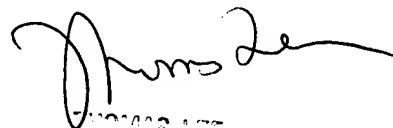
No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

(12) Conclusion

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,



CHUN CAO
CHUN CAO
PRIMARY EXAMINER


THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Conferees:

Thomas Lee

Lynne Browne


LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100